Multi-stage Motion Vector Prediction Schedule Strategy for AVS HD Encoder

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***Abstract*--Motion vector prediction (MVP) is a high-efficiency technology for motion estimation in video compressing. In this paper, a novel MVP schedule strategy is proposed for AVS HD real-time encoder. A multi-stage MVP architecture is designed in this strategy for the macroblock (MB)-based pipelining. The tradeoff between complexity and performance is achieved for the MVP architecture which breaks the data dependencies in the spatial MVP which is harmful for normal pipeline rhythm. The experimental results show that the proposed MVP schedule strategy meets the real-time requirement of AVS HD encoder with an acceptable coding performance loss.**

I. INTRODUCTION

AVS (Audio Video Coding Standard) HD encoder is implemented in FPGA supporting 720Px30fps HD video real-time encoding. Four-stages Macroblock (MB) pipeline architecture is designed for the HD encoder, including Integer pixel motion estimation (IME), Fractional motion estimation (FME), Mode decision (MD), and, Variable length coding (VLC). The encoder MB pipeline architecture is shown in Fig.1.

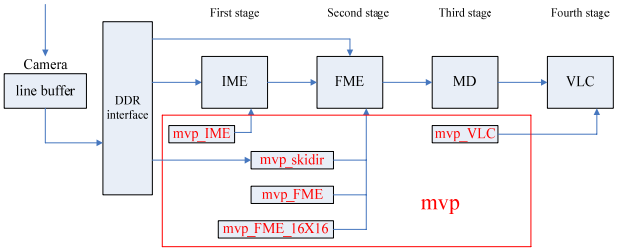


Fig. 1. AVS HD encoder architecture and MVP architecture

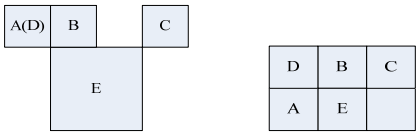
Motion vector prediction (MVP) is a high efficient technology for video coding. It is employed in several pipeline stages, such as IME, FME, MD, and VLC. The MVP is used to provide a start point of ME or a prediction of real MV. The calculation of MVP of current block is often dependent on the real MVs from its neighboring blocks. However, due to the MB-based pipeline architecture, the real MVs of neighboring blocks are not always available when MVP needs it. Some real MVs of neighboring blocks may be determined by next several stages. To break the MV dependencies in the MB-based pipeline architecture, MVP algorithm defined in standard is modified in some stages.

In this paper, the different MVP algorithms are used in different stages according to the pipeline architecture and the proposed multi-stage MVP schedule strategy is used to control the data communion, state transfer and MVP calculation. With the proposed MVP, the MVP dependency is efficiently alleviated with less performance loss.

II. MVP ALGORITHM AND SCHEDULE STRATEGY

A. MVP ALGORITHM

The relationship between current MB and neighboring block shows in Fig.2. If block C is existed, current block C will be predicted by the MV of A, B, and C, else, current block C will be predicted by the MVs of A, B, and D.



(a) (b)

Fig. 2. The relationship between current MB and neighboring block

1) MVP-IME

The results of analyzing and testing show that the neighboring candidate MVs selection for MVP has a small effect to the performance of IME. So an algorithm of MVP which has been simplified as MVP-IME is used in IME stage. MVP-IME will select MVs of top-left block A, top block B, and top-right block C for all modes[1]. It is showed above in Fig.2 (a).

2) MVP-FME

However, MVs selection for MVP has a significant effect to the performance of FME. MVP-IME which reduces the dependencies between MBs in pipeline doesn't feat any more. At the same time, also for avoiding the dependency relationship between MBs in pipeline, new algorithm for MVP called MVP-FME which has a proper complexity between MVP-standard and MVP-IME is used in FME stage.

If neighboring block is in the left MB of current MB (for example: block A in Fig.2 (b)), left MB is in MD pipeline stage. The best MV of neighboring block which will be chosen after MD pipeline hasn't existed. To satisfy the requirement of MB pipeline and get a good performance, the best MV is replaced by the result of FME with 8x8 mode.

If neighboring block is in the current MB (for example: block B in Fig.2 (b)), current MB is in FME pipeline stage. The best MV of neighboring block which will be chosen after MD stage hasn't existed. To meet the requirement of MB pipeline and get a good performance, because IME pipeline stage of current MB has finished, the best MV is replaced by the result of IME with 8x8 mode[2].

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3) MVP-standard

All the MVs are the best MVs. It is used in MVP-skidir and MVP-VLC, and MVP-standard.

B. MVP schedule strategy

According to the timing requirement of MB pipeline stages in MVP schedule strategy, five stages are designed in mvp architecture as shown in Fig.3.

(1) MVP of skip mode in P frame, and direct mode in B frame (MVP-skidir). MVP-skidir should start-up first. Because the result of FME-skidir will be used by MD in the same pipeline, the FME-skidir must do first. And FME-skidir needs the result of MVP-skidir, so MVP of the skip mode and the direct mode must start-up first. Then FME stage and MD stage won't be delayed. Time when MVP-skidir is finished has a great effect to the MB pipeline[3].

(2) MVP for all modes (except 16x16) in FME stage (MVP-FME). MVP-FME also needs to be finished fast, because in the same pipeline period, search of FME will use the results of MVP-FME.

(3) MVP for the best mode which be chosen in MD (MVP-VLC). When MVP-VLC is finished, data will be used by VLC in the same pipeline to write data, So, it should start-up the third.

(4) MVP for IME stage (MVP-IME). MVP-IME provides predicted MV for IME stage in next pipeline. It needn't to be finished quickly, so it starts-up the fourth.

(5) MVP for 16x16 mode in FME stage (MVP-FME_16x16). MVP-FME_16x16 provide predicted MV for FME stage in next pipeline, and needs to wait the 8x8 mode of FME in the current pipeline finished, So it starts-up at last.

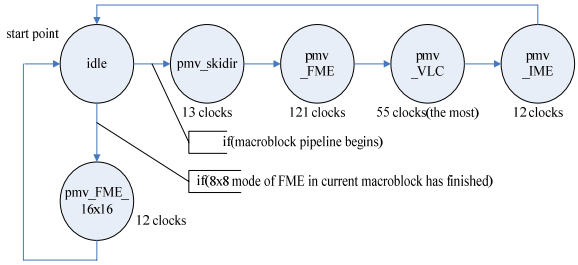

Fig. 3. MVP schedule strategy

The pipeline process of MVP in the whole MB pipeline of the encoder shows in the form below, achieving stabilization at 4T.

pipeline	T	2T	3T	4T	5T	6T	7T	8T	9T	10T	11T	12T	13T	14T
mvp-skidir			m0	m1	m2	m3	m4	m5	m6	m7	m8	m9	m10	
mvp-FME		m0	m1	m2	m3	m4	m5	m6	m7	m8	m9	m10		
mvp-VLC				m0	m1	m2	m3	m4	m5	m6	m7	m8	m9	m10
mvp-IME	m1	m2	m3	m4	m5	m6	m7	m8	m9	m10				
mvp-FME_16x16	m0	m1	m2	m3	m4	m5	m6	m7	m8	m9	m10			

Fig. 4. mvp pipeline

III. ANALYZING OF RESULTS

A comparison between the original MVP algorithm and the proposed multi-stage MVP is given to evaluate the performance degradation due to the proposed multi-stage MVP algorithm. In this test, 720p HD sequence Harbour is used. The results of test show below.

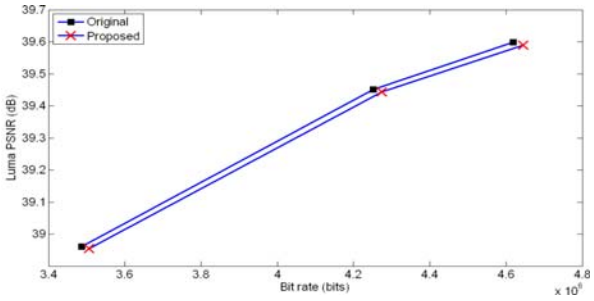

Fig. 5. The comparison between the original and the proposed multi-stage MVP

Multi-stage MVP schedule strategy has been implemented in verilog. It has been synthesized on Xilinx V5 LX330, and simulated successfully. Important data report synthesizing on Synplify shows below:

Register bits not including I/Os:	6940 (3%)
DSP48s:	16 of 192 (8%)
Global Clock Buffers:	1 of 32 (3%)
Estimated Frequency:	150 MHz
Total LUTs:	9914 (4%)

Fig. 6. the report of synthesizing on Synplify

The efficiency of the proposed motion vector prediction algorithm is verified by the results of the simulation and RTL synthesis. The multi-stage MB schedule strategy satisfies the requirement of MB pipeline, implements MVP quickly and effectively, and ensures that the HD encoder for AVS will be implemented successfully.

IV. CONCLUSION

Data dependency in MVP is harmful for normal hardware pipelining. Algorithm simplification for MVP is necessary for hardware implementation. In this work, we make a tradeoff between performance degradation and VLSI implementation complexity. The multi-stage MVP schedule strategy is well-suited for HD AVS encoder hardware implementation.

Reference

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