北京大学

硕士研究生学位论文

题目：AVS高清视频编码器运动矢量预测的研究与FPGA实现

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中文摘要

随着信息科学的进步，生活中人们对视频的需求也越来越普遍。视频本身连续生动，但有着信息量大的特点，为了便于传输和存储，必须要对视频进行压缩。目前国际上有着几种主流视频压缩标准，但是这些标准对使用者收取高昂的费用。AVS 标准是我国自主制定的第二代视频压缩的标准，在与 H.264 同等压缩效率的情况下，实现的复杂度却大大降低。同时能为使用者节省大量的标准负担。

研发出支持 AVS 标准的编解码芯片，将对标准的大规模产业化使用提供基础支撑。本人所在的实验室小组正在努力实现该编解码芯片。基于项目的支持，现阶段目标是在 FPGA 平台上首先验证实现支持 AVS 标准的高清实时视频编码器。

编码器硬件核中，各流程以流水的方式工作，基于宏块级别。由于运动矢量预测基于邻近块的运动矢量，这种相关性使得宏块顺序扫描时，宏块级流水会导致服务于多级流程的运动矢量预测具有一定的数据依赖，我们的编码器提出了一种新颖的 zig-zag 宏块扫描结构，在这种 zig-zag 结构下可以克服一定的数据依赖问题，相应的对算法也进行了调整。

运动矢量预测（MVP）是视频压缩运动估计中的关键模块，在运动估计压缩算法中是必不可少的，可以大幅提高压缩的效率。在这篇论文中，在新颖的 zig-zag 宏块扫描模式下，针对跨流水级的硬件结构，我们对标准中运动矢量预测算法进行了调整，解决了运动矢量预测中，对相邻块的数据依赖问题，同时性能只有很小的降低。将原有的基于一套运算电路的 MVP 硬件体系结构进行了拆分，节省了运算时间，使得流水线中各流程能够满足实时性下系统提出的约束。同时使某些数据的相关性在各流程内部处理，可以为未来硬件流水级的细分提供基础。实现中加入了相应的算法，使 MVP 模块支持 AVS 标准中制定的场编码模式。通过实现的结果表明，这种改进的 MVP 模块能够满足 AVS 高清编码器的实时需要，同时编码性能只有很小的降低，并将资源使用控制在可以接受的范围之内。

本论文第一章介绍了研究内容的背景内容和项目的实现目标，同时简要介绍了目前主流的一些视频压缩的标准，目的在于使读者能够对本论文的背景有一定的了解，以帮助读者更好的理解本论文的研究课题。

第二章，本论文将介绍 AVS 标准的一些情况，并在总体上对我们的编码器系统和芯片有一个介绍，这样对运动矢量预测模块在编码器芯片中的功能和位置有一个了解。

第三章会介绍 AVS 标准中制定的运动矢量预测的基本算法，随后将介绍在我们的系统中做运动矢量预测模块实现时对算法做出的调整。

第四章对运动矢量预测模块大的硬件实现做出分析，介绍了原有的整个运动矢量预测模块的结构设计，分模块对各级运动矢量的硬件实现进行介绍，之后简单介绍了模块拆分的情况。

第五章本论文给出了拆分前和拆分后仿真和综合的结果，同时对性能进行分析，表明该设计满足系统提出的设计约束，并对资源的使用情况作出对比。

第六章本论文描述了后续需要完成的工作，并对以后工作和研究领域发展趋势发表了自己的看法。

关键词：AVS，高清视频编码器，运动矢量预测，硬件实现结构，FPGA 平台

Motion Vector Prediction Research and Implementation for AVS HD Encoder Based on FPGA Platform

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Abstract

With the advances in information science andlife, people are increasingly demand for video-based applications. Continuous vivid video itself, but with informative features, in order to facilitate transmission and storage, the video must be compressed. Currently there exist several major international video compression standards, but these standards bring high cost to users. AVS standard is the second generation of self-developed video compression standard in China, compared to its counterpart of the international standard, H.264, AVS has similar compression efficiency but itsimplementation complexity is greatly reduced. Users can also save a lot on standard costs.

The video encoder chip which supports AVS standard will provide foundation for large-scale industrial use of AVS. Our laboratory team is working hard to implement the encoder chip. Based on a project, our current goal is verifing the encoder which achieves real-time high definition video encoding base AVS standard on FPGA platform.

The encoder hardware core is working in pipeline way based on the macro block level. Due to the motion vector prediction (MVP) based on motion vectors of neighboring blocks, this data dependence will make multi-pipeline level motion vector prediction can’t work. We proposed a new macroblock zag-zig scanning mode, in which we can solve some of the data dependences. The algorithm of MVP has been modified for the zag-zig scanning mode.

Motion vector prediction is the key module in video compression based on motion estimation. Motion vector prediction can significantly improve the compression efficiency. In this paper, based on new zig-zag scanning mode and multi-pipeline level hardware structure, we have modified the standard motion vector prediction algorithm to solve the data dependent problem.

We achieved it with a small reduction in performance of the encoder. We splited the original MVP hardware architecture to save computation time and make the pipeline to meet the real-time system's constraints. At the same time some data dependent problems will be put in module internal, that provide the basis for the segment of pipe-line level. Achieved by adding the corresponding algorithm, MVP module supports the field mode of AVS standard. The implementing results show that MVP meets the AVS real-time HD encoder needs with a small reduction in encoding performance, and the use of resources is in the acceptable range.

Chapter one, this paper firstly introduces the background of research content and goals of project. In same time it briefly introduces some of the current mainstream video compression standard to help readers better understand the research topic.

Chapter two, this paper describes some situations of the AVS standard, and introduction our encoder system and chip in general.

Chapter three, this paper introduces the basic algorithm of motion vector prediction in AVS standard, and our modifition of the motion vector prediction algorithm.

Chapter four, this paper introduced the original implement motion vector prediction module hardware architecture. Sub-module hardware implementation are introduced, followed by a brief introduction of the module after spliting.

Chapter five, this paper shows the results of simulation and synthesis, analyses of performance that made the design to meet system constraints and compares the use of resources.

Finally, the paper describes the follow-up needs to be done and the future development trend.

Keywords:HD video encoder, motion vector prediction, AVS, macroblock pipeline, RTL implement, FPGA platform